REMARKS

Below, the applicant's comments are preceded by related remarks of the examiner set forth in small bold font.

Claims 10-24 and 28-30 are rejected under 35 U. S. C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 is rejected based on lack of positive antecedent basis of "the coherency" and "the cache memory" on line 2.

The applicant has amended claim 10.

Claim 11 is rejected based on lack of positive antecedent basis of "the caching of system memory" on line 3; and "the content of the system memory they have cached" on line 6.

The applicant has amended claim 11.

Claim 12 is rejected because it is a process claim but it is claiming an apparatus of "a multi-port switch containing ports" on line 3. This renders the claim indefinite because it is not clear whether applicant is claiming a process or an apparatus.
Claims 13-19 are rejected because they depend on claim 12.

The applicant has amended claim 12.

Claim 19 is also rejected based on lack of positive antecedent basis of "the nodes requiring a cache update" on lines 5-6.

The applicant has amended claim 19.

Claim 20 is rejected because it is a process claim but it is claiming an apparatus of "a multi-port switch containing a plurality of ports" on line 3. This renders the claim indefinite because it is not clear whether applicant is claiming a process or an apparatus.
Claim 21 is rejected because it depends on claim 20.

The applicant has amended claim 20.

Claim 22 is rejected based on lack of positive antecedent basis of "the processor" on line 3.
Claims 23 and 24 are rejected because they depend on claim 22.

The applicant has amended claim 22.

Claim 28 is rejected because it is an apparatus claim but it is claiming several process limitations. This renders the claim indefinite because it is not clear whether applicant is claiming a process or an apparatus. Claims 29 and 30 are rejected because they depend on claim 28.

The applicant has amended claim 28.

Claims l-27 are rejected under 35 U. S. C. 102(b) as being anticipated by Sun Microsystems, Inc. (Sun), European, Patent Application EP 0 848 327 A2.

As per claim 1, Sun shows incorporating a multi-port switch into a multi-node computer system (at least in figs. 3-8 and throughout pages 2-3); and assigning at least a first port of the multi-port switch to a first domain of the nodes (page 2, lines 25-58). Sun shows all of the steps recited in claim 1.

The applicant has amended claim 1. As amended, claim 1 includes assigning at least a first port of a multi-port switch to a first domain of nodes and assigning at least a second port of the multi-port switch to a second domain of the nodes, the first domain of the nodes and the second domain of the nodes having separate and independent memory structures.

Sun divides a "common overall address space" to form domains or clusters within a system (page 4, line 55). "Clusters" allow multiple domains to share a common range of memory addresses (page 2, line 28). In an exemplary division of the common overall address space, the memory addresses run from '00 0000 0000' to '0F FFFF FFFF.' As shown in Fig. 3, "the address spaces of the clusters may overlap each other" (page 5, line 13). Thus, Sun divides a single unified memory into multiple ranges and does not describe or suggest a system having a first domain and a second domain that have separate and independent memory structures as in the applicant's claim 1.

As for claim 2...
As for claim 3...

Claims 2-3 are patentable for at least the same reasons as claim 1.

As for claim 4...

The applicant has canceled claim 4.

As for claim 5...
As for claim 6...

As for claim 7...
As for claim 8...
As for claim 9...
As for claim 10...
As for claim 11...

Claims 2-11 are patentable for at least the same reasons as claim 1.

As per claim 12, Sun shows providing a multi-port switch containing ports; and a first domain port assignment process for assigning at least a first port of said multi-port switch to a first domain (figs. 3-8 and pages 2-3 as noted above). Sun shows all of the elements recited in claim 12.

The applicant has amended claim 12. As amended claim 12 includes "a first domain port assignment process for assigning at least a first port of a multi-port switch to a first domain and a second domain port assignment process for assigning at least a second port of the multi-port switch to a second domain of the nodes, the first domain of the nodes and the second domain of the nodes having separate and independent memory structures." Sun does not disclose or suggest a system in which the first domain and the second domain have separate and independent memory structures.

As for claim 13...

Claim 13 is patentable for at least the same reasons as claim 12.

As for claim 14...

The applicant has canceled claim 14.

As for claim 15...
As for claim 16...
As for claim 17...
As for claim 18...
As for claim 19...

Claims 15-19 are patentable for at least the same reasons as claim 12.

Although claim 20 has been rejected based on indefiniteness under 35 USC Q 112, it is still being rejected based on the prior art under the assumption that it is a process claim and that there is a process step such as "providing a multiport switch containing ports " incorporated into the claim.

As per claim 20, Sun shows providing a multi-port switch containing a plurality of ports; and a port assignment process for assigning at least one port of said multi-port switch to one of a plurality of domains (figs. 3-8 and pages 2-3 as noted above). Sun shows all of the elements recited in claim 20.

The applicant has amended claim 20. As amended, claim 20 includes a port assignment process for assigning at least a first port of said multi-port switch to a first one of a plurality of domains and a second port assignment process for assigning at least a second port of the multi-port switch to a second one of a plurality of domains, the first one of a plurality of domains and the second one of a plurality of domains having separate and independent memory structures. Sun does not disclose or suggest a process in which the first domain and the second domain have separate and independent memory structures.

As for claim 21...

Claim 21 is patentable for at least the same reasons as claim 20.

As per claim 22, Sun shows a computer program product residing on a computer readable medium having a plurality of instructions stored thereon which, when executed by the processor, cause that processor to: assign at least a first port of a multi-port switch to a first domain; and route transactions, which are received by the multi-port switch and specify the first domain, to one or more ports assigned to the first domain (pp. 2-3 and 5, wherein the computer system "architecture " of Sun uses software to control its functions and operation of the domains and can quickly adjust the membership in the domains based on conditions or requirements). Sun shows all of the elements recited in claim 22.

The applicant has amended claim 22. As amended claim 22 includes instructions to assign at least a first port of a multi-port switch to a first domain and assign at least a second port of the multi-port switch to a second domain, the first domain and the second domain having separate and independent memory structures. Sun does not describe or suggest such a process in which the first domain and the second domain have separate and independent memory structures.

As for claim 23...

Claim 23 is patentable for at least the same reasons as claim 22.

As per claim 25, Sun shows a processor and memory configured to: assign at least a first port of a multi-port switch to a first domain; and route transactions, which are received by the multi-port switch and specify the first domain, to one or more ports assigned to the first domain (pages 2-3 and 5). Sun shows all of the elements recited in claim 25.

The applicant has amended claim 25. As amended, claim 25 includes a system configured to assign at least a first port of a multi-port switch to a first domain and assign at least a second port of the multi-port switch to a second domain, the first domain and the second domain having separate and independent memory structures. Sun does not describe or suggest a process in which the first domain and the second domain have separate and independent memory structures.

As for claim 26...
As for claim 27...

Claims 26 and 27 are patentable for at least the same reasons as claim 25.

As per claim 28, Kumar et al. (Kumar) shows a multi-port switch containing a plurality of ports (275); a IO hub controller connected to one of said ports (280); a scalable node controller (120) connected to one of said ports; at least one microprocessor (127) connected to said scalable node controller. Kumar does not specifically show a first domain port assignment means for assigning at least a first port of said multi-port switch to a first domain; and a first domain transaction routing means for routing transactions, which are received by said multi-port switch and specify the first domain, to one or more ports assigned to the first domain. However, as noted above Sun does show a first domain port assignment means for assigning at least a first port of said multi-port switch to a first domain; and a first domain transaction routing means for routing transactions, which are received by said multi-port switch and specify the first domain, to one or more ports assigned to the first domain (pp. 2-3 and 5). It would have been obvious to one of ordinary skill in the art at the time of the invention to include the domain partitioning of Sun in the system of Kumar in order to isolate the elements of the computer system into independent units so that if any particular domain encounters errors or problems the rest of the system can still operate with not difficulty (as noted on page 2 of Sun).

The applicant has amended claim 28. As amended, claim 28 includes a domain partitioning system configured to include a first domain port assignment process for assigning at least a first port of said multi-port switch to a first domain and a second domain port assignment

process for assigning at least a second port of the multi-port switch to a second domain of the nodes, the first domain and the second domain having separate and independent memory structures. As described above, Sun does not describe or suggest such a process in which the first domain and the second domain have separate and independent memory structures . In addition, Kumar does not disclose or suggest multiple domains having separate and independent memory structures. Thus, whether taken alone or in combination with Kumar claim 1 would not have been obvious.

As for claim 29...

The applicant has canceled claim 29.

As for claim 30...

Claim 30 is patentable for at least the same reasons as claim 28.

The fact that the applicant has addressed certain positions of the examiner in this response should not be construed as a concession with respect to any other positions of the examiner. The fact that the applicants have made certain arguments for the patentability of certain claims should not be construed as a concession by the applicant that there are not other good reasons for the patentability of those claims or other claims.

Respectfully submitted,

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